Claims

1. A method for operating a pipelined microprocessor, said method including steps for

detecting a first instruction that stores to a first memory location, said first instruction including syntax for computing an effective address for said first memory location;

detecting a second instruction that stores to a second memory location, said second instruction including syntax for computing an effective address for said second memory location;

determining, in response to said syntax for said first instruction and said syntax for said second instruction, a relationship between said first memory location and said second memory location, without computing said effective address for both said first memory location and said second memory location; and

determining whether to perform one of said first instruction and second instruction in response to said step of determining a relationship.

Add A7